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Appl. No.	:	10/737,247	Confirmation No. 5845
Applicant	:	William POHLMAN et al	
Filed	:	12/15/2003	
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Examiner	:	VU, BAO Q	
Docket No.	:	P-001D	
Customer No.	:	34398	

Title: APPARATUS FOR PROVIDING REGULATED POWER TO AN INTEGRATED CIRCUIT

APPEAL BRIEF

Dear Sir/Madam:

This is a brief for an appeal from a Final Office Action mailed February 21, 2006, and pursuant to a Notice of Appeal that was timely filed on May 22, 2006. The Appeal Brief Fee of $ 500.00 in accordance with 41.20(b)(2) is enclosed herewith.

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I. REAL PARTY IN INTEREST

The real party in interest in this appeal is the assignee of this application, PRIMARION, Inc.

II. RELATED APPEALS AND INTERFERENCES

Appellant is unaware of any related appeals or interferences.

III. STATUS OF THE CLAIMS

The application was originally filed with Claims 1-18. Claims 1-18 remain pending and all stand rejected. This is an appeal of rejected Claims 1-18. Claims 1-18 are reproduced and attached in the Claims Appendix.

IV. STATUS OF AMENDMENTS

Applicants submitted a response to the non-final office action dated October 17, 2005. These claims were finally rejected in the Final Office Action. The 18 claims that appear before the Board are those 18 claims that were originally filed and re-submitted in unamended form in the response to the non-final office action dated October 17, 2005. These claims 1-18 are attached hereto in the Claims Appendix.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Claim 1 is directed to a tiered power regulation system 100 (FIG. 1). (For the sake of convenience, references to the drawing figures and the specification are made with respect to US Patent Number 6,429,630; which is the parent patent application that issued with the same drawings and specification as the instant application, and is attached herewith as Appendix B - US PATENT 6,429,630 - PARENT OF APPLICATION.) See FIG. 1 illustrating a first power regulator 110, an array 120 comprising a plurality of second power regulators 120(a) – 120(n), said second power regulators configured to respond to a load power demand rate greater than said first power regulator responds to power demands, (See the specification at e.g. col. 4 lines 49-54 noting that time delays associated with larger regulators are mitigated because smaller regulators within an array are used to provide current to a portion or portions of the microprocessor.) wherein said array 120 comprising a plurality of second power regulators 120(a) – 120(n), is configured to couple to a plurality of portions of a microprocessor 130 (FIG. 1).

Claims 2-8 are dependent claims and all depend directly from claim 1. Claim 2 specifies that the regulator array 120 is coupled to the microprocessor 130 using bump technology (col. 4 line 66). FIG. 3 refers to using a compound semiconductor substrate (page 5 line 5-19). Claim 4 specifies a switching regulator (col. 3 line 30). Claim 5 recites the second power regulators 120 being coupled together in parallel (FIG. 1). Claim 6 recites the first regulator 210 providing power to said array 220 and to said microprocessor 230 (FIG. 2). Claim 7 recites electronic components 150 coupled to said microprocessor 130, said components configured to provide

power to said microprocessor 130. Claim 8 recites said array 220 coupled in parallel to said first regulator 210 and to said microprocessor 130 (FIG.2).

Claim 9 is directed to a tiered power regulation system. See FIG. 1 illustrating a first power regulator 110, a microelectronic device 130 formed on a first substrate and an array 120 of second power regulators (120(a)-120(n) configured to respond to a load power demand rate greater than said first power regulator 110 responds to power demands. (See the specification at e.g. col. 4 lines 49-54 noting that time delays associated with larger regulators are mitigated because smaller regulators within an array are used to provide current to a portion or portions of the microprocessor.) Claim 9 further recites that the microprocessor device and array of second power regulators are on two different substrates.

Claims 10-17 are dependent claims that depend directly from claim 9. Claim 10 is directed to bump technology (col. 4 line 66). Claim 11 recites the case where the first power regulator is a Buck regulator (col. 3 line 34). Claim 12 recites that the microelectronic device comprises a microprocessor. Claim 13 is directed to the second substrate comprising compound semiconductor material (col. 2 line 22).. Claim 14 is directed to the second power regulators 120 being coupled together in parallel (FIG. 1). Claim 15 recites that the first regulator 210 provides power to the array 220 and to the microelectronic device 230 (FIG. 2). Claim 16 further recites electronic components 250 coupled to said microelectronic device 230, said components 250 configured to provide power to said microelectronic device 230 (FIF. 2). Claim 17 recites the array 220 coupled in parallel to said first regulator 210 and to said microelectronic device 230 (FIG.2).

Claim 18 is the third independent claim directed to a tiered power regulation system

comprising: a first power regulator 110, a microelectronic device 130 formed on a first substrate and an array of second power regulators 120 formed on a second substrate, said second power regulators configured to respond to a load power demand rate (See the specification at e.g. col. 4 lines 49-54 noting that time delays associated with larger regulators are mitigated because smaller regulators within an array are used to provide current to a portion or portions of the microprocessor.) greater than said first power regulator responds to power demands; wherein said array is coupled in parallel to said microelectronic device 130 using bump technology (col. 4 line 66).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The grounds of rejection to be reviewed on appeal are as follows:

1) Claims 1-18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Blish U.S. Patent No. 5,914,873 in view of U. S. Patent No. 5,938,769 to HU.

VII. APPELLANT'S ARGUMENT

A. Claims 1-18 Are Patentable Over Blish in view of Hu

The Examiner has rejected Claims 1-18 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,914,873 to Blish (hereinafter "Blish") in view of Hu U.S. Patent No. 5,938,769. *Final Office action at pages 2-4.*

The Board should overturn this rejection because Blish does not teach or suggest every element recited in each of the claims, because Hu does not teach the claim elements missing from the teachings of Blish, because there is no motivation or suggestion to modify Blish in accordance with Hu and because even if Bllish were modified in accordance with Hu, appellant's invention would be neither anticipated nor rendered obvious in the sense of 35USC103.

1. Summary of Blish

Blish discloses a distributed voltage converter for high power microprocessor with array connections. *See Title.* In this regard, Examiner has referenced voltage converters 220(a), 220(n) supplying power to a microprocessor silicon chip comprising an array of logic gates 210. *See column 6 lines 19-21 and FIG. 4.* Since no mention in Bliss is made to the contrary, it is presumed that all the regulators provide current to the microprocessor as well as the logic gates at the same speed. Blish is not concerned with the speed with which currents are provided because a response to transient events is a problem not addressed or solved by the power supply design of Blish.

2. Comparison of Applicants' Device v. Blish

At best, *arguendo* the voltage converters 220(a), 220(n) of Blish *See FIG. 4* can be analogized with array 120 of applicants' invention *See FIG. 1.* Blish has no further relevance. Blish does not teach a tiered power regulation system that proposes a first power regulator 110 in

addition to array 120 coupled to a microprocessor. *See FIG 1.* Since Blish does not teach tiered power regulation, *a fortiori,* Blish does not teach one regulator responding to a load power demand rate greater than the other power regulator. Applicants recognized the need to respond to the transient power demands of electronic devices (such as a microprocessor) by: "supplying electronic devices with relatively high, regulated current at relatively high speed". *See col. 2 lines 2-4, and col. 2 lines 47-48. See also col. 2 line 65* "short response time", *col. 3 line 43* "rapid response power transfer", *col. 3, line 42* "low response time (e.g. at speeds of 500 MHz and above)", etc.

Applicants also recognized the technical difficulties of one power supply performing the functions of supplying current at such a high demand rate as well as overall power demands. For this reason, they invented the tiered power regulation system comprising both a first power regulator and a second array.

In the final rejection, Examiner correctly notes that: "The claim language clearly states that the second power demand rate is greater than that of the first demand rate" (emphasis added) *See page 3 of the Office Action.* However, then Examiner incorrectly concludes that: "There is no distinguishing difference between applicants' claim language and that of the prior art." In fact, even if one were to attribute the prior art with the ability to provide different power levels (as for example by the various embedded voltage converters 220(a), 220(n) *See Fig. 4 of Blish,* this is patentably distinct from Applicants' tiered power regulation system. Applicants' invention provides not only array 120 for satisfying a high demand rate but also intermediate power regulator 110. *See Fig. 1.* As another embodiment, Applicants connect intermediate regulator 210 in parallel with array 220 to load device 230. *See Fig. 2* and this is also not shown in Blish. Neither the problem addressed by Applicants (satisfying microprocessors' power needs including the total power

requirements as well as the need for fast response to demand rate) nor the solution of using a tiered power regulation system are taught by Blish.

Examiner did conclude that: "Blish discloses the claimed device except to having differing load power demand rates"(emphasis added) *See page 2 of the Office Action.* As noted above, Applicants disagree with Examiner's contention that Blish discloses the claimed tiered power regulation system of Applicants. However, Applicants agree with Examiner that Bilsh does not disclose differing power demand rates. In order to overcome the shortcomings of the Blish reference as noted by Examiner, Examiner cited Hu.

3. Summary of Hu

Hu discloses a CPU escalating adapter with multivoltage and multiple frequency selection. *See the Abstract.* Basically, Hu recognized that a CPU can operate at different frequencies and requires different power levels. In accordance with Hu's disclosure: a toggle actuator has a plurality of switches connected with an input of multiple frequency selection of the CPU for providing a function of selecting frequency multiplication factors. *See Col 2 lines 11-13.* In short, a higher level of power is provided when the CPU operates at a higher frequency. However, Hu is not a tiered power regulation system. Hu never discusses or contemplates the use of two power supplies where one provides power at a faster response time than the other. Hu is not concerned with the speed with which currents are provided because a response to transient events is a problem not addressed or solved by the power supply design of Hu.

4. Comparison of Applicants' Device v. Hu

At best, *arguendo,* Hu discloses that: "With a combination of the voltage regulator 30, the stabilivolt integrated circuit 40, the divider resistor 41 ant the toggle switch member 70, output

voltage of the voltage regulator 30 can be changed..." *See Fig. 1 and col. 3, lines 12-15.* In other words, a different power level is supplied to the CPU for different clock speeds of operation. It would appear that Examiner contends that this teaching of different power levels supplied to a microprocessor capable of operating at different clock frequencies adds to the teachings of Bliss and renders Applicants' invention obvious.

However, the presetting of switches for the application of different levels of power has absolutely no relationship to supplying power satisfying a high demand rate. Pre-setting switches merely establishes the level of power to be supplied for the particular clock frequency of operation. On the other hand, the power demand rate is primarily a function of the speed at which the demand for current changes as the number of active gates changes depending on the type of operation being performed by a microprocessor. In a particular section of the microprocessor (e.g. the arithmetic logic unit – commonly referred to as ALU), the power demand might be low when suddenly the demand becomes great. In other words, while only a few gates in a section of the microprocessor are active at one instant, many (if not all) gates are turned on demanding more power. Applicants realized that while one power regulator might be optimized to provide normal power requirements, it would not be optimized for the case when the load power demand changed quickly. For this reason, Applicants provide a tiered power regulation system where the second power regulators can be optimized to handle this transient condition. Applicants' array 220 is configured to respond to this transient "load power demand" at a "rate greater than the first power regulator 210 responds to power demands" (by microelectronic device 230) *See Fig. 2.* Thus, neither Bliss nor Hu, either singly or in combination teach Applicants' invention. When neither of two cited references teaches Applicants' invention then the combination of the two references cannot render the invention obvious in the sense of 35 U.S.C. 103.

5. Claim 1 is directed to a tiered power regulation system comprising a first power regulator and an array comprising a plurality of second power regulators, said second power regulators configured to respond to a load power demand rate greater than said first power regulator responds to power demands

Claim 1 is directed to a tiered power regulation system comprising a first power regulator and an array comprising a plurality of second power regulators, said second power regulators configured to respond to a load power demand rate greater than said first power regulator responds to power demands, wherein said array is configured to couple to a plurality of portions of a microprocessor. The first of the tiered power regulators respond to the regular power demands of the load. The second power regulators respond to a load power demand rate greater than said first regulator responds to power demands.

(a) Examiner's rejection of Claim 1

The Examiner has rejected claim 1 as being obvious over Blish in view of Hu. In particular, the Examiner asserts that: "Blish describes an array of voltage regulators (220a-220n) connected in parallel and having a first voltage regulator that accepts a first power demand that is lower than the second power demands which would be greater. After noting that Blish does not teach: "having differing load power demand rates", Examiner states that: "Hu discloses that it is known in the art to provide having differing load power demand rates. It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide an array of voltage regulators (220a-220n) connected in parallel of Blish with the provide a having differing load power demand rates of Hu, in order to provide a more diversified and power supply system capable of handling load and power demands of the circuit." *See the Final Office Action at page 2.* Examiner has inserted: "differing load power demand rate" from Applicants'

claims as there is no such teaching in Hu. Moreover there is no suggestion in either Blish or Hu why or how the two references could be combined to raise a question of obiousness.

(b) Legal Standard for a prima facie case of obviousness

To establish a *prima facie* case of obviousness, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings, and the prior art reference must teach or suggest all the claim limitations. M.P.E.P. § 2143. Also, the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991). Since the final rejection does not meet this legal standard, it should be reversed on this basis alone.

(c) There is No Suggestion or Motivation for the Modification of Blish by the teachings of Hu.

The Examiner has failed to point to any suggestion or motivation in the prior art to modify Blish in view of Hu. It is well-settled that "a showing of a suggestion, teaching, or motivation to combine [or modify] the prior art references is an 'essential component of an obviousness holding'." *C.R. Bard, Inc. v. M3 Systems, Inc.*, 157 F.3d 1340, 1352 (Fed. Cir. 1998). In addition, the mere fact that the prior art may be modified in the manner suggested by the examiner does not make the modification obvious unless the prior art suggested the desirability of the modification. *In re Fritch, 972 F.2d 1260, 1266 n. 14, 23 USPQ2d 1780,1783-4 n.14 (Fed Cir. 1992); In re Gordon, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984)*

In the Final Office Action, the Examiner has simply argued that "..it would have been obvious to one having ordinary skill in the art at the time of the invention was made to provide

an array of voltage regulators (220a-220n) connected in parallel of Blish with the provide of having differing load power demand rates of Hu, in order to provide a more diversified and power supply system capable of handling load and power demands of the circuit" *Final Office Action, page 2.* The Examiner has pointed to no objective teaching in either Blish or Hu for such an assertion, nor has the Examiner identified any basis as to why a person of ordinary skill in the art would be motivated to modify Blish in view of Hu. Because the Examiner has failed to point to any evidence of record showing a motivation to modify Blish in view of Hu, the Examiner has failed to satisfy the burden of showing *prima facie* obviousness of Blish in view of Hu. The Board should overturn the rejection of Claim 1 on this basis alone.

(d) Neither Bllish nor Hu Teach or Suggest all of the claim limitations of claim 1. Therefore, even if Blish were properly modifiable in view of Hu, the resultant structure, mode of operation and result would not render Claim 1 obvious in the sense of 35 USC 103.

Blish does not teach or suggest all of the claim limitations of claim 1. In particular, Blish does not teach or suggest "A tiered power regulation system comprising a first power regulator and an array comprising a plurality of second power regulators, said second power regulators configured to respond to a load power demand rate greater than said first power regulator responds to power demands, wherein said array comprising a plurality of second power regulators is configured to couple to a plurality of portions of a microprocessor (emphasis added). As noted hereinabove in Section VII A2 and VII A 4 comparing Applicants' device to the teachings of Blish and Hu, these significant elements in the combination of Applicants' invention are missing from both Blish and Hu. When none of the cited references teach or suggest important aspects of Applicants' claimed invention, the combination of two references cannot be said to raise a question of obviousness. This would be the case, even if the two

references were properly combined (which they are not). For the reasons set forth in this paragraph alone, the Board is respectfully requested to reverse the Examiner's rejection of claim 1.

6. Claims 2-8

Claims 2-8 all depend directly from Claim 1. Therefore, Claims 2-8 include all the limitations of Claim 1. The Board should overturn the Examiner's rejection of Claims 2-8 at least for the reasons expressed with respect to Claim 1, which are incorporated by reference. The rejection of claims 2-8 should also be overturned because claims 2-8 recite additional features. The additional features are more specific recitation of how the first power regulator and plurality of second power regulators are configured so that the array of second power regulators responds to a power demand rate greater than the first power regulator. For example, claim 2 recites bump technology. Claim 3 recites a compound semiconductor substrate (inherently faster response than a device on a silicon substrate). Claim 4 recites a switching regulator. Claim 5 recites the second power regulators being coupled in parallel. Claim 6 recites the first regulator providing power to both the array and to the microprocessor. Claim 7 recites components configured to provide power to the microprocessor. Claim 8 recites the array coupled in parallel to said first regulator and to said microprocessor. *See Fig. 2 showing a configuration contemplated neither by Blish nor Hu.* These features are not taught or suggested by Blish or Hu. Therefore, the rejection of claims 2-8 should be overturned by the Board for the same reasons as claim 1 and also because claims 2-8 recite additional features.

7. Claim 9 recites "a tiered power regulation system where the array of second power regulators are configured to respond to a load power demand rate greater than said first power regulator responds to power demands"

Claim 9, like claim 1 recites a tiered power regulation system where the array of second power regulators are configured to respond to a load power demand rate greater than said first power regulator responds to power demands. In addition, claim 9 recites that while the microelectronic device is formed on a first substrate the array of second power regulators are formed on a second substrate. These features are not taught or suggested by Blish or Hu. Therefore, the rejection of claim 9 should be overturned by the Board for the same reasons as claim 1 (the claim 1 patentability position being incorporated herein) and also because claim 9 recites additional features.

8. Claims 10-17

Claims 10-17 depend directly from Claim 9. Therefore, Claims 10-17 include all the limitations of Claim 9. The Board should overturn the Examiner's rejection of Claims 10-17 at least for the reasons expressed with respect to Claim 9, which is incorporated by reference. The rejection of claims 10-17 should also be overturned because claims 10-17 recite additional features. The additional features are more specific recitation of how the first power regulator and plurality of power regulators are configured so that the second power regulators respond to a power demand rate greater than the first power regulator. For example, claim 10 recites bump technology. Claim 11 recites a Buck regulator. Claim 12 specifies a microprocessor. Claim 13 recites a compound semiconductor material (inherently faster response than a device on a silicon substrate). Claim 14 recites that the second power regulators are coupled together in parallel. Claim 15 recites that the first regulator provides power to the array and to the microelectronic

device. Claim 16 recites electronic components configured to provide power to the microelectronic device. Claim 17 recites the array coupled in parallel to said first regulator and to said microprocessor. *See Fig. 2 showing a configuration contemplated neither by Blish nor Hu.* In the overall combination, the features recited in claims 10-17 are not taught or suggested by Blish or Hu. Therefore, the rejection of claims 10-17 should be overturned by the Board for the same reasons as claim 9 and also because claims 10-17 recite additional features.

9. Claim 18 recites "a tiered power regulation system where the array of second power regulators are configured to respond to a load power demand rate greater than said first power regulator responds to power demands, as well as first and second substrates"

Claim 18, like claim 9 recites a tiered power regulation system where the array of second power regulators are configured to respond to a load power demand rate greater than said first power regulator responds to power demands, as well as first and second substrates. In addition, claim 18 recites that the microelectronic device is formed on the first substrate and wherein the array is coupled in parallel to the microelectronic device using bump technology. In the overall combination, these features are not taught or suggested by Blish or Hu. Therefore, the rejection of claim 18 should be overturned by the Board for the same reasons as claim 1 and claim 9 and also because claim 18 recites additional features.

B. Conclusion

In view of the foregoing arguments, Claims 1-18 are patentable over Blish, US Patent 5,914,873 in view of Hu US Patent 5,938,769..

Respectfully submitted,

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CLAIMS APPENDIX

1. (Original) A tiered power regulation system comprising:

a first power regulator; and

an array comprising a plurality of second power regulators, said second power regulators configured to respond to a load power demand rate greater than said first power regulator responds to power demands,

wherein said array comprising a plurality of second power regulators is configured to couple to a plurality of portions of a microprocessor.

2. (Original) The tiered power regulation system of claim 1, wherein said regulator array is coupled to said microprocessor using bump technology.

3. (Original) The tiered power regulation system of claim 1, wherein said regulator array is formed using a compound semiconductor substrate.

4. (Original) The tiered power regulation system of claim 1, wherein said first regulator is a switching regulator.

5. (Original) The tiered power regulation system of claim 1, wherein said second power regulators are coupled together in parallel.

6. (Original) The tiered power regulation system of claim 1, wherein said first regulator provides power to said array and to said microprocessor.

7. (Original) The tiered power regulation system of claim 1, further comprising electronic components coupled to said microprocessor, said components configured to provide power to said microprocessor.

8. (Original) The tiered power regulation system of claim 1, wherein said array is coupled in parallel to said first regulator and to said microprocessor.

9. (Original) A tiered power regulation system comprising:

a first power regulator;

a microelectronic device formed on a first substrate; and

an array of second power regulators formed on a second substrate, said second power regulators configured to respond to a load power demand rate greater than said first power regulator responds to power demands.

10. (Original) The tiered power regulation system of claim 9, wherein said microelectronic device and said array are coupled together using bump technology.

11. (Original) The tiered power regulation system of claim 9, wherein the first power regulator is a Buck regulator.

12. (Original) The tiered power regulation system of claim 9, wherein the microelectronic device comprises a microprocessor.

13. (Original) The tiered power regulation system of claim 9, wherein the second substrate comprises compound semiconductor material.

14. (Original) The tiered power regulation system of claim 9, wherein said second power regulators are coupled together in parallel.

15. (Original) The tiered power regulation system of claim 9, wherein said first regulator provides power to said array and to said microelectronic device.

16. (Original) The tiered power regulation system of claim 9, further comprising electronic components coupled to said microelectronic device, said components configured to provide power to said microelectronic device.

17. (Original) The tiered power regulation system of claim 9, wherein said array is coupled in parallel to said first regulator and to said microelectronic device.

18. (Original) A tiered power regulation system comprising:

a first power regulator;

a microelectronic device formed on a first substrate; and

an array of second power regulators formed on a second substrate, said second power regulators configured to respond to a load power demand rate greater than said first power regulator responds to power demands,

wherein said array is coupled in parallel to said microelectronic device using bump technology.

EVIDENCE APPENDIX

NONE

RELATED PROCEEDINGS APPENDIX

NONE